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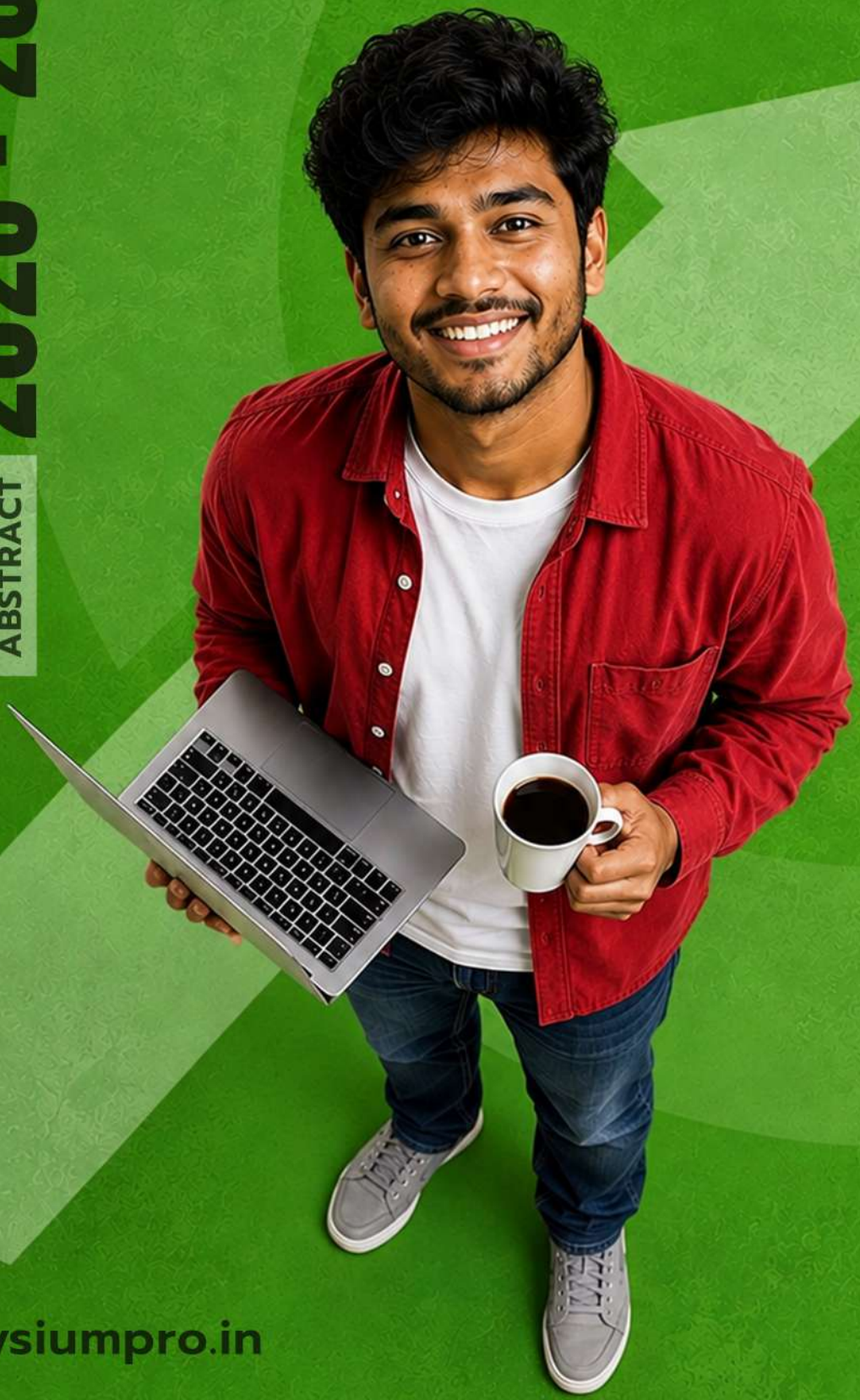
2026 - 2027

TITLE & ABSTRACT

Advanced Academic Final Year Projects



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A 90.9-dB SNDR Fourth-Order Fully Passive Bandpass Current-Integrating Noise-Shaping SAR Light-to-Digital Converter

This project presents the design of a high-resolution light-to-digital converter based on a fourth-order fully passive bandpass current-integrating noise-shaping SAR architecture. The proposed design combines current integration, noise-shaping techniques, and successive approximation register (SAR) conversion to achieve a high signal-to-noise-and-distortion ratio (SNDR) of 90.9 dB. The fully passive loop filter reduces power consumption and circuit complexity while improving conversion efficiency and accuracy. The architecture effectively suppresses quantization noise and enhances dynamic range for precise optical signal measurement. This VLSI-based converter is suitable for low-power, high-performance sensing applications in advanced optical and biomedical systems.

TABv2: A Faster Ternary and Binary Neural Network Inference Library on the Edge

This project presents TABv2, an optimized inference library designed for faster execution of ternary and binary neural networks on edge computing platforms. The proposed framework focuses on reducing computational complexity and memory requirements by utilizing low-bit neural network operations. Efficient hardware-aware optimization techniques are applied to improve inference speed while maintaining accuracy in resource-constrained environments. The library enables energy-efficient deep learning applications by minimizing data movement and accelerating bit-level computations. TABv2 is suitable for edge AI applications such as real-time image processing, embedded vision, and intelligent IoT systems.

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Design Space Exploration of a Unified FPGA Accelerator for Elliptic-Curve-Based Functions in Attribute-Based Encryption

This project focuses on the design and optimization of a unified FPGA accelerator for implementing elliptic-curve-based cryptographic functions used in attribute-based encryption (ABE) systems. The proposed architecture explores different design parameters to achieve an effective balance between performance, area utilization, and power efficiency. A hardware acceleration approach is developed to improve the execution speed of complex elliptic curve operations such as point multiplication and modular arithmetic. The design space exploration process evaluates various FPGA architectures to identify optimized configurations for secure and efficient cryptographic processing. The proposed accelerator is suitable for high-performance security applications including cloud computing, IoT devices, and privacy-preserving communication systems.

Real-Time Proximity Sensing for Autonomous Systems: Custom AFE and FPGA Acceleration for FMCW Architecture

This project presents a real-time proximity sensing system for autonomous applications using a frequency-modulated continuous-wave (FMCW) architecture with a custom analog front-end (AFE) and FPGA-based acceleration. The proposed design integrates signal acquisition, processing, and distance estimation techniques to achieve fast and accurate object detection. A dedicated AFE circuit improves signal conditioning by providing efficient amplification, filtering, and noise reduction for received FMCW signals. FPGA acceleration enables high-speed digital processing and real-time computation while reducing latency and power consumption. The proposed VLSI-based architecture is suitable for advanced autonomous systems, robotics, automotive sensing, and intelligent monitoring applications.

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Headsail: One-Year Tape-Out of a 25-mm² Linux-Capable RISC-V MPSoC

This project focuses on the design and successful tape-out of a 25-mm² Linux-capable RISC-V multi-processor system-on-chip (MPSoC) named Headsail. The proposed architecture integrates multiple RISC-V processor cores, memory subsystems, and dedicated hardware components to support efficient embedded computing and operating system execution. The design process emphasizes rapid development, optimized area utilization, and high-performance system integration within a compact silicon footprint. Advanced VLSI design methodologies are applied to achieve reliable functionality, low power consumption, and scalable processing capability. The developed MPSoC provides a flexible platform for edge computing, embedded Linux applications, and next-generation intelligent systems.

60-Gb/s 1:4 Demultiplexer in 22-nm FD-SOI Technology Using TSPC Logic: A Circuit-to-System-Level Analysis and Design

This project presents the design and analysis of a high-speed 60-Gb/s 1:4 demultiplexer implemented using true single-phase clock (TSPC) logic in 22-nm fully depleted silicon-on-insulator (FD-SOI) technology. The proposed architecture focuses on achieving high data throughput with improved speed, power efficiency, and reduced circuit complexity. A detailed circuit-to-system-level analysis is performed to evaluate the performance of the demultiplexer for advanced high-frequency communication applications. The use of TSPC logic enables efficient clocking, reduced delay, and enhanced signal integrity at high operating frequencies. This VLSI design is suitable for next-generation optical communication systems, high-speed data interfaces, and advanced semiconductor applications.

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RRAM-Based Spectral-Domain Convolution Accelerator for Reliable and Energy-Efficient CNN Inference

This project presents an RRAM-based spectral-domain convolution accelerator designed to improve the performance and energy efficiency of convolutional neural network (CNN) inference. The proposed architecture utilizes resistive random-access memory (RRAM) technology to perform in-memory computing, reducing data movement between processing units and memory. A spectral-domain convolution approach is employed to accelerate complex neural network operations while maintaining high computational accuracy and reliability. The design focuses on achieving low power consumption, faster processing speed, and improved hardware efficiency for edge AI applications. This VLSI-based accelerator is suitable for energy-efficient deep learning systems, intelligent IoT devices, and next-generation artificial intelligence platforms.

Overflow-Driven Dynamic Precision Scaling Fixed-Point Multiply-Accumulator Unit

This project presents an overflow-driven dynamic precision scaling fixed-point multiply-accumulator (MAC) unit designed for efficient VLSI computing applications. The proposed architecture dynamically adjusts computational precision based on overflow detection to optimize power consumption and hardware utilization. By scaling the precision according to data requirements, the design reduces unnecessary computation while maintaining numerical accuracy and system performance. The MAC unit incorporates efficient multiplication and accumulation operations suitable for digital signal processing and machine learning workloads. This energy-efficient VLSI design is applicable to low-power artificial intelligence accelerators, embedded processors, and high-performance computing systems.

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A 10-Gb/s NRZ/PAM-4 Compatible Transceiver Using 8b/10b Recovery for Automotive Applications

This project presents a high-speed NRZ/PAM-4 compatible transceiver designed for automotive communication systems. The architecture uses 8b/10b encoding and recovery techniques to improve signal integrity and reduce transmission errors. The proposed design achieves reliable data communication with high bandwidth and low power consumption. The VLSI implementation focuses on improving speed, efficiency, and robustness for automotive networking applications.

HardVault: A Hybrid FPGA-Based Ethereum-Bitcoin Cold Wallet

This project presents HardVault, a hybrid FPGA-based secure hardware wallet for Ethereum and Bitcoin cryptocurrency protection. The design combines FPGA acceleration with security mechanisms to perform cryptographic operations efficiently. The architecture provides enhanced data protection, fast transaction processing, and resistance against cyber threats. This VLSI-based solution is suitable for secure blockchain and digital asset storage applications.

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HiePlace: Efficient Hierarchical PCB Placement

This project focuses on an efficient hierarchical PCB placement methodology to optimize electronic system design. The proposed approach improves component placement accuracy, reduces routing complexity, and enhances design efficiency. Hierarchical optimization techniques are used to achieve better area utilization and signal performance. The system is suitable for advanced PCB and VLSI design automation applications.

QuickCell: Fast Automatic Design of Standard Cells for Silicon Dangling Bond Logic

This project presents QuickCell, an automated standard cell design framework for silicon dangling bond logic circuits. The proposed method accelerates cell generation and optimization while improving design efficiency. The architecture focuses on reducing development time and enhancing circuit performance. This approach supports future nanoscale VLSI technologies and advanced logic implementations.

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Continual Learning-Guided Adaptive Approximate Computing for Real-Time MEA Spike Detection

This project introduces an adaptive approximate computing technique for real-time microelectrode array (MEA) spike detection. The design uses continual learning methods to improve processing efficiency while maintaining detection accuracy. Approximate computing reduces hardware complexity and power consumption. The proposed VLSI architecture is suitable for biomedical signal processing and neural monitoring applications.

A 0.2%-THD Sinusoidal Signal Generator With First-Order Analog Interpolation Over More Than Three Frequency Decades for EIS Applications

This project presents a low-distortion sinusoidal signal generator using first-order analog interpolation techniques. The design achieves 0.2% total harmonic distortion (THD) across a wide frequency range. The proposed architecture provides accurate signal generation with improved linearity and efficiency. It is suitable for electrochemical impedance spectroscopy and precision analog applications.

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EVMx: An FPGA-Based Accelerator for Smart Contract Processing

This project presents EVMx, an FPGA-based accelerator designed for efficient smart contract execution. The architecture improves blockchain processing speed by accelerating Ethereum Virtual Machine operations. FPGA implementation provides parallel processing capability with reduced latency and power consumption. The proposed system is suitable for high-performance blockchain applications.

A Review of Bandwidth Enhancement Techniques for Die-to-Die Single-Ended Interfaces in Chiplets

This project reviews various bandwidth enhancement techniques for die-to-die single-ended interfaces used in chiplet-based systems. The study analyzes signal integrity, communication speed, and power efficiency improvements. Different architectural approaches are compared for advanced semiconductor integration. The review supports the development of high-speed chiplet communication technologies.

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Vertically Stacked Doping-Less Dual-Metal Gate Nanosheet FET With TiO2 Dielectric for High Sensitivity Autoimmune Disease Biosensing

This project presents a vertically stacked doping-less dual-metal gate nanosheet FET for highly sensitive biosensing applications. The use of TiO2 dielectric improves electrical characteristics and sensing performance. The proposed transistor structure enhances sensitivity and reduces leakage current. This nano-VLSI device is suitable for advanced biomedical detection systems.

Machine Learning-Driven Prediction of Optimal Design Parameters for Ripple Carry Adder

This project applies machine learning techniques to predict optimal design parameters for ripple carry adders. The proposed approach reduces design exploration time and improves circuit optimization. ML-based prediction helps achieve better speed, power, and area trade-offs. The method is useful for efficient arithmetic circuit design in VLSI systems.

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A Comparative Study of Attention-Based Transformer and Deep CNN Architectures for Lithography Hotspot Detection in Advanced Process Nodes

This project compares transformer-based attention models and deep CNN architectures for lithography hotspot detection. The study evaluates accuracy, complexity, and computational efficiency for advanced semiconductor manufacturing. Machine learning techniques are used to improve defect prediction. The approach supports reliable and efficient VLSI fabrication processes.

Full Precision Hardware Implementation of the AlphaEvolve 4×4 Complex Valued Matrix Multiplication Algorithm

This project presents a full precision hardware implementation of the AlphaEvolve 4×4 complex matrix multiplication algorithm. The architecture focuses on improving computational accuracy and processing efficiency. Optimized hardware design reduces execution time for complex mathematical operations. The proposed system is suitable for AI accelerators and signal processing applications.

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Impact of MAC Unit Design Architectures and Their Applications in Modern Computing: An In-Depth Review

This project provides an in-depth review of different multiply-accumulate (MAC) unit architectures used in modern computing systems. Various designs are analyzed based on speed, power consumption, and hardware efficiency. The study highlights MAC optimization techniques for AI and DSP applications. The review supports future low-power processor and accelerator designs.

Dual-Mode CMOS LIF Neuron With Subthreshold Efficiency and Saturation-Driven Robustness

This project presents a dual-mode CMOS leaky integrate-and-fire (LIF) neuron circuit with improved energy efficiency. The design operates in subthreshold mode for low power consumption and uses saturation-based techniques for robustness. The proposed architecture enhances neural computation efficiency. It is suitable for neuromorphic VLSI and brain-inspired computing systems.

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99447 93398

info@elysiumpro.in

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229, First Floor, A Block,
Elysium Campus,
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Madurai, Tamil Nadu -
625020.

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