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CADANCE

Advanced Academic Final Year Projects

2026 - 2027

TITLE & ABSTRACT

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MACHINE LEARNING

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Impact of MAC Unit Design Architectures and Their Applications in Modern Computing

This project focuses on designing and analyzing different Multiply-Accumulate (MAC) unit architectures using Cadence Virtuoso. Various transistor-level circuit structures are implemented and evaluated for power, delay, area, and energy efficiency. The designs are simulated under different operating conditions to compare their computational performance. Layout implementation can be performed to verify physical design characteristics and parasitic effects. The study helps identify efficient MAC architectures for low-power digital signal processing and modern computing applications.

A Comprehensive Survey of Custom Layout Techniques for 6T, 8T, and 10T SRAM Bitcells

This project investigates custom layout techniques for 6T, 8T, and 10T SRAM bitcells across different CMOS technology approaches. SRAM schematics are designed and simulated using Cadence Virtuoso to evaluate stability, power, delay, and read/write characteristics. Custom layouts are developed and checked using Design Rule Check and Layout Versus Schematic verification. Cell area and performance are compared across the different SRAM architectures. The study supports the selection of suitable SRAM structures for low-power memory applications.

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Low Power and Highly Stable 10T SRAM Cell Design Using Stacked and MTCMOS Techniques

This project develops a low-power and highly stable 10T SRAM cell using transistor stacking and MTCMOS techniques. The SRAM circuit is designed at transistor level using Cadence Virtuoso and evaluated during read, write, and hold operations. Power consumption, static noise margin, leakage current, and access delay are measured through simulations. The layout is implemented and verified using standard physical-design checks. The proposed design aims to improve SRAM stability and energy efficiency for low-power VLSI systems.

0.5 V BD-MIMO DDTA-Based Universal Multimode Biquad Filter

This project designs a low-voltage universal multimode biquad filter using a differential difference transconductance amplifier architecture. Cadence Virtuoso is used to implement the circuit at transistor level with a 0.5 V supply. Different filter responses such as low-pass, high-pass, band-pass, and notch characteristics are simulated. Frequency response, power consumption, linearity, bandwidth, and operating range are analyzed. The design targets low-power analog and mixed-signal applications.

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Four-Quadrant CMOS Analog Multiplier Using Digital Inverter Standard Cells

This project investigates the implementation of a four-quadrant CMOS analog multiplier using digital inverter standard cells. The circuit is designed and simulated at transistor level using Cadence Virtuoso. Multiplication accuracy, linearity, bandwidth, power consumption, and output swing are evaluated through simulations. Different input amplitudes and operating conditions are applied to validate four-quadrant multiplication. The approach explores a compact and reusable architecture for analog computation in mixed-signal systems.

Axial Ratio Improvement for Wide-Angle Scanning Circularly-Polarized Phased Array

This project focuses on improving the axial ratio of a circularly polarized phased-array antenna through circuit and RF simulation techniques. The antenna and associated RF structures can be modeled and analyzed using suitable Cadence RF design tools. Different phase and amplitude conditions are evaluated to improve polarization characteristics during beam scanning. Parameters such as gain, axial ratio, impedance matching, and radiation response are analyzed. The design supports compact RF front-end and wireless communication applications.

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Low-Voltage Mixed-Mode Analog Filter Using Multiple-Input Multiple-Output OTAs

This project develops a low-voltage mixed-mode analog filter using multiple-input multiple-output operational transconductance amplifiers. The circuit is designed at transistor level using Cadence Virtuoso with emphasis on low supply voltage operation. Frequency response, bandwidth, power consumption, linearity, and filter characteristics are simulated. Different input configurations can generate multiple filtering responses from the same circuit. The design is suitable for low-power analog and mixed-signal signal-processing applications.

A Novel Hybrid RF-DC Converter Using CMOS n-Well Process

This project designs a CMOS-based hybrid RF-to-DC converter for harvesting energy from radio-frequency signals. The circuit is implemented and simulated using Cadence Virtuoso with a CMOS n-well process. Rectification, voltage conversion, output power, conversion efficiency, and sensitivity are analyzed under different RF input conditions. Transistor sizing and circuit parameters are optimized to improve low-input-power performance. The proposed design can support low-power wireless and energy-harvesting applications.

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Low-Voltage Current-Mode Analog Filter Using Current Differencing Transconductance Amplifier

This project develops a low-voltage current-mode analog filter based on a current differencing transconductance amplifier. The circuit is designed at transistor level using Cadence Virtuoso and optimized for low power consumption. Frequency response, bandwidth, current gain, linearity, and power consumption are evaluated through simulations. Different filter responses can be achieved by modifying circuit configurations and passive components. The design is suitable for compact low-voltage analog signal-processing systems.

An Error Bound Particle Swarm Optimization for Analog Circuit Sizing

This project develops an optimization-based approach for transistor sizing in analog circuits using Particle Swarm Optimization. Cadence Virtuoso is used to simulate the analog circuit and generate performance parameters such as gain, bandwidth, power, and noise. An error-bound optimization algorithm searches for transistor dimensions that satisfy predefined circuit specifications. Optimized designs are validated through Cadence simulations and compared with conventional sizing methods. The approach reduces manual design effort and improves analog circuit performance.

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Low-Power, Low-Energy, Static, Contention-Free TSPC Dual-Edge Triggered Flip-Flops

This project designs a low-power dual-edge triggered flip-flop using true single-phase clocking techniques. The circuit is implemented at transistor level using Cadence Virtuoso and analyzed for power, delay, and energy consumption. Static and contention-free operation is evaluated under different input and clock conditions. Layout implementation can be performed to analyze area and post-layout performance. The design is suitable for energy-efficient digital VLSI and high-speed processor applications.

A Novel 18T Hybrid Master-Slave Flip-Flop With Low Power and Delay

This project develops an 18-transistor hybrid master-slave flip-flop optimized for low power and propagation delay. Cadence Virtuoso is used to design and simulate the transistor-level circuit. Setup time, hold time, clock-to-Q delay, power consumption, and energy-delay characteristics are evaluated. Different input switching and clock frequencies are tested to verify reliable operation. The proposed flip-flop targets low-power and high-performance digital VLSI systems.

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Ultra-Low-Power Fully-Static Contention-Free Single-Phase-Clock Flip-Flop With Low Area

This project develops an ultra-low-power fully static flip-flop using a single-phase clock architecture. The circuit is implemented using Cadence Virtuoso and optimized for low transistor count, low power, and compact area. Timing characteristics such as setup time, hold time, propagation delay, and clock-to-Q delay are analyzed. Power consumption is evaluated across different operating frequencies and supply voltages. The design is suitable for energy-efficient digital circuits and low-power processors.

Business-Aware SLA-Driven Autoscaling for Kubernetes Microservices Using Application-Level Observability

This project develops an intelligent autoscaling framework for containerized microservices based on application-level performance metrics. Monitoring data such as response time, workload, resource utilization, and service-level agreement parameters are analyzed. Machine learning or rule-based prediction can determine suitable scaling decisions according to changing workloads. The system dynamically adjusts service resources to maintain performance while reducing unnecessary resource usage. The approach supports efficient and reliable cloud-native application management.

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Device and Circuit Level Performance of Vertically Stacked Doping-Less Nanosheet Field Effect Transistor

This project investigates the device and circuit-level performance of vertically stacked doping-less nanosheet FET structures. Device characteristics are analyzed through suitable semiconductor simulation and transistor-level circuit modeling. Parameters such as threshold voltage, leakage current, drive current, switching behavior, and power consumption are evaluated. The device can be incorporated into basic digital circuits for comparison with conventional transistor technologies. The study explores nanosheet transistor technology for future low-power VLSI systems.

58-nW 0.5-V Mixed-Mode Universal Filter Using Multiple-Input Multiple-Output OTAs

This project develops an ultra-low-power universal filter operating at a 0.5 V supply voltage. Multiple-input multiple-output OTAs are designed at transistor level using Cadence Virtuoso. The filter supports different responses such as low-pass, high-pass, band-pass, and band-stop operation. Power consumption, frequency response, bandwidth, linearity, and output characteristics are analyzed. The design targets battery-operated biomedical, IoT, and low-power mixed-signal applications.

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0.3-V 36-nW Voltage-Mode First-Order Filter Based on Multiple-Input OTA

This project develops an ultra-low-voltage first-order voltage-mode filter using a multiple-input operational transconductance amplifier. The circuit is designed and simulated in Cadence Virtuoso with a 0.3 V supply. Frequency response, cutoff frequency, power consumption, linearity, and output swing are evaluated. Transistor sizing and biasing conditions are optimized to achieve stable operation at very low power. The proposed filter is suitable for energy-constrained sensor and biomedical circuits.

Low-Voltage Current-Mode Analog Filter Using Current Differencing Transconductance Amplifier

This project implements a low-voltage current-mode analog filter using a current differencing transconductance amplifier. Cadence Virtuoso is used for transistor-level schematic design and circuit simulation. Filter frequency response, bandwidth, current gain, power consumption, and linearity are evaluated. The circuit is optimized for low supply voltage and reduced power consumption. The design can be used in low-power communication, sensor-interface, and mixed-signal applications.

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Ultra-Low-Power and Fast-Locking Injection-Locked CDR in 18-nm FinFET Technology

This project develops an injection-locked clock and data recovery circuit using an advanced FinFET technology node. Cadence Virtuoso is used for transistor-level design and simulation of the CDR architecture. Locking time, recovered clock quality, jitter, power consumption, frequency range, and data recovery performance are analyzed. Circuit parameters are optimized to achieve fast locking with minimal energy consumption. The design targets next-generation IoT and high-speed communication systems.

A 42.5 nW, 0.5 V Differential Difference Transconductance Amplifier and Its Application in Low-Power Universal Filter

This project designs an ultra-low-power differential difference transconductance amplifier operating at a 0.5 V supply. The DDTA is implemented and simulated using Cadence Virtuoso at transistor level. Important parameters including transconductance, gain, bandwidth, power consumption, linearity, and output swing are evaluated. The amplifier is integrated into a universal filter to demonstrate its analog signal-processing capability. The proposed design is suitable for low-power biomedical, IoT, and mixed-signal applications.

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