FINAL YEAR PROJECTS
VLSI 2017-2018
TITLES WITH ABSTRACTS

CALL US @ 994-479-3398, (0452) 4390702
18 Years of Experience • Automated Services • 24/7 Help Desk Support
Advanced Technologies And Tools • Legitimate Members Of all Journals
Timing error resilience is a promising alternative to eliminate margins and improve energy efficiency in subthreshold and near-threshold processors. However, the existing techniques have some limitations, such as uncontaminated architecture registers (ARs), strict timing constraints on error consolidation and propagation, and high design complexity. To address these limitations, a new timing error resilience technique based on sacrificial instruction-level registers is proposed. It dynamically captures and incrementally records the changes of ARs at each instruction boundary. Once a timing error occurs, it only needs to restore the changed ARs to a preerror state. Then, the erroneous instruction can be safely reexecuted. This technique is applicable to different processors. The 32-bit embedded processor employing the proposed technique is demonstrated in a 40-nm CMOS technology. This variation-tolerant processor operates at 27.4 MHz under 0.6 V with 8.7% total area overhead compared with the baseline without timing error resilience. At the same throughput, the proposed technique achieves 44% and 27% energy benefits compared with the baseline and the canary technique, respectively.

This paper presents a digitally controlled 2-/3-phase 6-ratio switched-capacitor (SC) dc-dc converter with low output voltage ripple and high efficiency. To achieve wide input and output voltage ranges, six voltage conversion ratios are generated with only two discrete flying capacitors by using both 2- and 3-phase operations. An adaptive ripple reduction scheme is proposed to achieve up to four times reduction in the output voltage ripple. The complexity of controller design is reduced by using digital synthesis, and the technique is scalable with process. Fast loop response is achieved by using synchronized hysteretic control. The SC converter was fabricated in a 0.13-μm CMOS process. It can deliver a maximum power of 250 mW to an output of 0.5–3 V with a wide input voltage range of 1.6–3.3 V. Compared to an SC converter with only 2-phase operation, the maximum efficiency improvement is 20%. The converter achieves a peak efficiency of 91%.
This paper introduces a sudden power-outage resilient in-processor check pointing for energy-harvesting non-volatile processors. In energy harvesting applications, a power supply generated from a renewable power source is unstable that may induce frequent sudden power outages, causing the inconsistency among distributed non-volatile flip-flops (NVFFs) and hence failure rollbacks in conventional non-volatile processors. To realize continuous operations upon the frequent sudden power outages, the proposed in-processor check pointing technique fixes the inconsistency using time-reminding redundant NVFFs (TM-RNVFFs). The TM-RNVFFs store the current and the past few data with the timing information of storing. If several NVFFs fail to store the current data due to the sudden power outages, the proposed in-processor check pointing technique exploits the timing information to find the common newest state among distributed NVFFs, leading to correct rollbacks to the state with consistency. The sudden power-outage effect is modelled to perform design space explorations at different configurations, such as redundancy and check pointing period. Non-volatile ARM Cortex-M0 processors are designed using hybrid 90 nm CMOS and 70 nm magnetic tunnel junction (MTJ) technologies. Based on the design space explorations, the proposed non-volatile processor achieves a several order-of magnitude reduction in rollback error probability with a power dissipation overhead of 11.6 percent and an area overhead of 52.1 percent in comparison with the conventional non-volatile processor.

A low-power ultrawideband (UWB) pulse generator based on pulsed oscillator architecture for 3-5 GHz applications is proposed. The pulsed oscillator is improved, so it realizes binary phase shift keying (BPSK) modulation. Unlike ON-OFF keying or pulse-position modulation (PPM), BPSK can scramble the spectrum, so it can be used in high pulse rate applications without having spectral line problem. The signal structure in this design is burst mode of PPM+BPSK. The proposed UWB pulse generator was successfully implemented on 0.18-μm CMOS technology. The peak-to-peak amplitude of output pulse is about 220 mV with 50-Ω load, the maximum power consumption is 4 mW at a raw data rate of 7.8 Mbps and the energy consumption is 32 pJ/pulse at a pulse rate of 125 Mpulses/s.
Continuous shrinking of the size of CMOS technology leads to extremely fast devices, but the resulting interconnect structures impose so many parasitic effects that the advantage of extremely scaled and ultrahigh-speed transistors would be completely overshadowed if appropriate remedial steps are not taken. This requires an accurate and efficient estimation of interconnect parasitics and analysis of their impact on integrated circuit performance. This paper proposes a new delay model for RLC interconnect networks in CMOS technology based on a second order approximate transfer function. The proposed modeling approach includes all possible scenarios (complex poles, real poles, and double poles) in the interconnect model. Simulation results show that the proposed delay model is almost independent of the ratio of \( V_{out}/V_{in} \), and the driver resistance has significant impact on the delay. The simulation results also show that the real pole model provides better accuracy and is much faster than the complex pole model. This observation would help to optimize the values of interconnect parasitics for faster operation.

This paper presents a novel class H power amplifier aiming for audio applications on battery-powered electronic devices. The power supply of the amplifier is adaptively adjusted to track the instantaneous input signal amplitude for higher power efficiency. By embedding audio input signal amplitude information into the class AB amplifier’s output common-mode voltage level, the amplifier is able to operate with only single-rail power supply and demonstrates more smooth transitions between the light load and heavy load mode, hence achieves lower total harmonic distortion (THD) for a wide load range. Fabricated in the AMS 0.18-\( \mu \)m CMOS process, the chip consumes 3.52 mW quiescent power and is able to deliver 526 mW peak output power to a 16 \( \Omega \) load. The measurement results indicate that the amplifier incurs no deterioration on THD when entering the supplytracking mode and achieves a lowest THD+N ratio of −80 dB. The peak power efficiency of the system is 80.4%; moreover, it demonstrates significant higher efficiency for medium load range compared to other linear mode amplifiers.
In this brief, a novel two-extra-column trellis min-max algorithm and the decoder architecture based on only the first minimum values are proposed for nonbinary low-density parity-check (NB-LDPC) codes. The algorithm greatly reduces the hardware complexity and improves the latency as well as the throughput of the proposed decoder architecture compared with the previous works. A layered decoder architecture based on the proposed algorithm for (837, 726) NB-LDPC code over GF(32) is implemented with a 90-nm CMOS technology. The results show a decrease in the area of 24.6% for the check node unit and 75.6% for the whole decoder with a throughput of 1.27 Gb/s. The proposed decoder provides a lower area and a higher efficiency compared with the state of the art of high-rate NB-LDPC codes with high Galois-field order.

An eight-stage reconfigurable charge pump for microelectromechanical system (MEMS) electrostatic actuation was designed and fabricated in a standard 0.13-μm CMOS technology. The purpose of the circuit is to generate sufficient on-chip voltages that are continually reconfigurable for MEMS actuation. Small 1-pF pumping capacitors are used to reduce the circuit area. Digitally programmable voltage levels can be outputted by varying the number of stages and the clock drive levels dynamically. Reduced power consumption is achieved using a variable frequency clock. The circuit attains a measured maximum output voltage of 10.1 V from a 1.2 V supply. Its nominal clock is set to 50 MHz. The circuit has a compact area of 215 μm × 300 μm and consumes 864 μW at a 50-MHz clock and 252 μW at an 8-MHz clock.
Very large-scale integrated circuit design, based on today's CMOS technologies, are facing various challenges. Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based design can resolve the issue of leakage power and bring the advantage of nonvolatility. However, radiation-induced soft error is still an issue in such new designs as they need peripheral CMOS components. As a result, these magnetic-based circuits are still susceptible to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike regardless of the induced charge. Besides, our MFA circuit offers a lower energy consumption in write operation as compared with previous counterparts. We also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full nonvolatility for future non-volatile microprocessors.

Two low power-delay-product (PDP) dynamic CMOS circuit design techniques are proposed. The techniques can simply modify existing dynamic CMOS designs to improve dynamic circuit delay and PDP. Conventional benchmark circuits and the modified circuits using the proposed techniques are implemented in 90 nm CMOS technology with a 1.2 V power supply. Simulation results indicate that the proposed techniques can improve circuit PDP by 19.2 and 61.9% in two non-inverted dynamic benchmarks, respectively, and 6.2 and 33.72% in two inverted dynamic benchmarks, respectively.
VLSI realizations of digit-recurrence binary division usually use redundant representation of partial remainders and quotient digits. The former allows for fast carry-free computation of the next partial remainder, and the latter leads to less number of the required divisor multiples. In studying the previous relevant works, we have noted that the binary carry-save (CS) number system is prevalent in the representation of partial remainders, and redundant high radix representation of quotient digits is popular in order to reduce the cycle count. In this paper, we explore a design space containing four division architectures. These are based on binary CS or radix-16 signed digit (SD) representations of partial remainders. On the other hand, they use full or partial precomputation of divisor multiples. The latter uses smaller multiplexer at the cost two extra adders, where one of the operands is constant within all cycles. The quotient digits are represented by radix-16 [-9, 9] SDs. Our synthesis-based evaluation of VLSI realizations of the best previous relevant work and the four proposed designs show reduced power and energy figures in the proposed designs at the cost of more silicon area and delay measures. However, our energy-delay product is 26%-35% less than that of the reference work.

The Montgomery algorithm is a fast modular multiplication method frequently used in cryptographic applications. This paper investigates the digit-serial implementations of the Montgomery algorithm for large integers. A detailed analysis is given and a tight upper bound is presented for the intermediate results obtained during the digit-serial computation. Based on this analysis, an efficient digit-serial Montgomery modular multiplier architecture using carry save adders is proposed and its complexity is presented. In this architecture, pipelined carry select adders are used to perform two final tasks: adding carry save vectors representing the modular product and subtracting the modulus from this addition, if further reduction is needed. The proposed architecture can be designed for any digit size \( \delta \) and modulus \( \theta \). This paper also presents logic formulas for the bits of the precomputation \(-0^{-1} \mod 2^\delta\) used in the Montgomery algorithm for \( \delta \leq 8 \). Finally, evaluation of the proposed architecture on Virtex 7 FPGAs is presented.
A conditional-boosting flip-flop is proposed for ultralow-voltage application where the supply voltage is scaled down to the near-threshold region. The proposed flip-flop adopts voltage boosting to provide low latency with reduced performance variability in the near-threshold voltage region. It also adopts conditional capture to minimize the switching power consumption by eliminating redundant boosting operations. Experimental results in a 65-nm CMOS process indicated that the proposed flip-flop provided up to 72% lower latency with 75% less performance variability due to process variation, and up to 67% improved energy-delay product at 25% switching activity compared with conventional precharged differential flip-flops.

Current mode is a popular CMOS-based implementation of threshold logic functions, where the gate delay depends on the sensor size. This paper presents a new implementation of current mode threshold functions for improved gate delay and switching energy. An analytical method is also proposed in order to identify quickly the sensor size that minimizes the gate delay. Simulation results on different gates implemented using the optimum sensor size indicate that the proposed current mode implementation method outperforms consistently the existing implementations in delay as well as switching energy.
An efficient multi-rate encoder for IEEE 802.16e LDPC codes which outperforms current single rate encoders with acceptable hardware consumption and efficient memory consumption is proposed. This design utilizes the common dual-diagonal structure in parity matrices to avoid the inverse matrix operation which requires extensive computations. Parallel Matrix-vector multiplication (MVM) units, bidirectional operation and storage compression are applied to this multi-rate encoder to increase the encoding speed and significantly reduce the quantity of memory bits required. The proposed encoding architecture also contributes to the design of multi-rate encoders whose parity matrices are dual-diagonally structured and have an Approximately lower triangular (ALT) form, such as in IEEE 802.11n and IEEE 802.22. Simulation results verified that the proposed encoder can efficiently work for all code rates specified in WIMAX standard. With a maximum clock frequency of 117 MHz, the encoder achieves 3 to 10 time’s higher throughput than prior works. The proposed encoder is capable to switch among six rates by adjusting the input parameter and it achieves the throughput up to 1Gbps.

Quasi-cyclic low-density parity-check (QC-LDPC) codes are adopted in many digital communication and storage systems. The encoding of these codes is traditionally done by multiplying the message vector with a generator matrix consisting of dense circulant submatrices. To reduce the encoder complexity, this paper introduces two schemes making use of finite Fourier transform. We focus on QC-LDPC codes whose circulant submatrices are of dimension \((2^r - 1) \times (2^r - 1)\) and the entries are elements of \(\text{GF}(2^p)\), where \(p\) divides \(r\), and hence, \(\text{GF}(2^p)\) is a subfield of \(\text{GF}(2^r)\). These cover a broad range of codes, and binary LDPC codes are a special case. Making use of conjugacy constraints, low-complexity architectures are developed for finite Fourier and inverse transforms over subfields in this paper. In addition, composite field arithmetic is exploited to eliminate the computations associated with message mapping and reduce the complexity of Fourier transform. For a \((2016, 1074)\) nonbinary QC-LDPC code whose generator matrix consists of circulants of dimension \(63 \times 63\) with \(\text{GF}(2^2)\) entries, the proposed encoders achieve 22% area reduction compared with the conventional encoders without sacrificing the throughput.
Low density parity check (LDPC) lattices were the first family of lattices equipped with iterative decoding algorithms. We introduce quasi-cyclic LDPC (QC LDPC) lattices as a special case of LDPC lattices with one binary QC-LDPC code as their underlying code. These lattices are obtained from the Construction A of lattices providing us to encode them efficiently using shift registers. To benefit from an encoder with linear complexity in the lattice dimension, we obtain the generator matrix of these lattices in quasi-cyclic form. We generalize the proposed quasi-cyclic form of the generator matrix for other Construction A lattices, namely the LDA lattices, with a non-binary QC-LDPC code as their underlying code. We provide a low-complexity decoding algorithm of QC LDPC-lattices based on the sum product algorithm. To design lattice codes, QC LDPC-lattices are combined with the nested lattice shaping that uses the Voronoi region of a sublattice for shaping. The shaping gain and the shaping loss of our lattice codes with dimensions 40, 50, and 60 using an optimal quantizer, are presented. The guidelines for applying efficient shaping methods, like hypercube shaping, for QC LDPC-lattices are also given. Consequently, we establish a family of lattice codes that perform practically close to the sphere bound.

This study represents designing and implementation of a low power and high speed 16 order FIR filter. To optimise filter area, delay and power, different multiplication techniques such as Vedic multiplier, add and shift method and Wallace tree (WT) multiplier are used for the multiplication of filter coefficient with filter input. Various adders such as ripple carry adder, Kogge Stone adder, Brent Kung adder, Ladner Fischer adder and Han Carlson adder are analysed for optimum performance study for further use in various multiplication techniques along with barrel shifter. Secondly optimisation of filter area and delay is done by using add and shift method for multiplication, although it increases power dissipation of the filter. To reduce the complexity of filter, coefficients are represented in canonical signed digit representation as it is more efficient than traditional binary representation. The finite impulse-response (FIR) filter is designed in MATLAB using equiripple method and the same filter is synthesised on Xilinx Spartan 3E XC3S500E target field-programmable gate array device using Very High Speed Integrated Circuit Hardware Description Language (VHDL) subsequently the total on-chip power is calculated in Vivado2014.4. The comparison of simulation results of all the filters show that FIR filter with WT multiplier is the best optimised filter.
Sequences of randomly generated bipartite configurations are analyzed; under mild conditions almost surely such configurations have minimum bisection width proportional to the number of vertices. This implies an almost sure $\Omega(n^2/d_{\text{max}}^2)$ scaling rule for the energy of directly implemented low-density parity-check (LDPC) decoder circuits for codes of block length $n$ and maximum node degree $d_{\text{max}}$. It also implies an $\Omega(n^{3/2}/d_{\text{max}})$ lower bound for serialized LDPC decoders. It is also shown that all (as opposed to almost all) capacity-approaching, directly-implemented non-split-node LDPC decoding circuits, have energy, per iteration, that scales as $\Omega(\chi^2 \ln^3 \chi)$, where $\chi = (1 - R/C)^{-1}$ is the reciprocal gap to capacity, $R$ is code rate, and $C$ is channel capacity.

---

The positive-feedback gain-enhancement operational transconductance amplifier (OTA) design is a promising architecture to scale into deep submicron CMOS. Ever smaller CMOS process nodes require analog circuit designs that can overcome the area–power-matching relation. We introduce a Nauta OTA with a split architecture consisting of fixed width and digitally programmable variable width transconductors utilizing the minimum grid-spacing of the CMOS process enabling an active mismatch cancelation technique. A variation-aware statistical design practice is introduced to analyze the sizing of transconductors, computing code-word solutions for statistically likely solutions, and estimating average maximum dc gain over the entire code-space of many simulated OTAs. Prototypes of a 8-bit differential OTA in 180-nm CMOS designed using the Nauta structure fixed width and digitally programmable variable width architecture achieves an average maximum dc gain of 60 dB, simulated unity gain frequency of 4.6 GHz, and a figure-of-merit of 1 GHz/mW.
In this paper, a CMOS chlorophyll concentration detector based on organic chlorophyll battery for measuring vegetable chlorophyll concentration is newly proposed. The organic chlorophyll battery and analog processing circuits are compactly and robustly cooperated. Comparing with previous works, the proposed chlorophyll concentration detector can be possibly easy and low-cost realized by users. All the functions and performance of the proposed chlorophyll concentration detector for measuring vegetable chlorophyll concentration are successfully tested and proven through measurements. The measured chlorophyll concentration of spinach ranges from 25 to 475 μmol/m², and the corresponding output frequency range is 599.2 kHz-1.174 MHz. The proposed chlorophyll concentration detector is suitable for devices measuring vegetable chlorophyll concentration.

In this paper, a novel radiation-hardened-by-design (RHBD) 12T memory cell is proposed to tolerate single node upset and multiple-node upset based on upset physical mechanism behind soft errors together with reasonable layout-topology. The verification results obtained confirm that the proposed 12T cell can provide a good radiation robustness. Compared with 13T cell, the increased area, power, read/write access time overheads of the proposed 12T cell are -18.9%, -23.8%, and 171.6%/-50.0%, respectively. Moreover, its hold static noise margin is 986.2 mV which is higher than that of 13T cell. This means that the proposed 12T cell also has higher stability when it provides fault tolerance capability.
<table>
<thead>
<tr>
<th>ETPL VLSI - 023</th>
<th>A High-Efficiency 6.78-MHz Full Active Rectifier with Adaptive Time Delay Control for Wireless Power Transmission.</th>
</tr>
</thead>
<tbody>
<tr>
<td>This paper presents a full active rectifier consisting of GaN devices and a CMOS controller designed for wireless power transmission in high-power consumer devices. An adaptive time delay control circuit is developed to maximize the conduction interval of the GaN switch, which can significantly reduce the power loss caused by the forward voltage imposed by the diode. The proposed control algorithm also eliminates the reverse leakage current of the rectifier, and thus further improves its power transfer efficiency. The controller implemented based on a high-voltage 0.18-μm CMOS process and the power stage consisting of four GaN transistors are assembled on the same printed circuit board (PCB) board. The proposed rectifier provides a maximum output current of 3 A at 5 V, with a 6.78-MHz ac input voltage. Its peak power transfer efficiency is 91.8%.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ETPL VLSI - 024</th>
<th>Design of Defect and Fault-Tolerant Non-volatile Spintronic Flip-Flops.</th>
</tr>
</thead>
<tbody>
<tr>
<td>With technology down scaling, static power has become one of the biggest challenges in a system on chip. Normally off computing using nonvolatile (NV) sequential elements is a promising solution to address this challenge. Recently, many NV shadow flip-flop architectures have been introduced in which magnetic tunnel junction (MTJ) cells are employed as backup storing elements. Due to the emerging fabrication processes of magnetic layers, MTJs are more susceptible to manufacturing defects than their CMOS counterparts. Moreover, unlike memory arrays that can effectively be repaired with well-established memory repair and coding schemes, flip-flops scattered in the layout are more difficult to repair. Therefore, without effective defect and fault tolerance for NV flip-flops, the manufacturing yield will be affected severely. In this paper, we propose a fault-tolerant NV latch (FTNV-L) design, in which several MTJ cells are arranged in such a way that it is resilient to various MTJ faults. The simulation results show that our proposed FTNV-L can effectively tolerate all single MTJ faults with a considerably lower overhead than traditional approaches.</td>
<td></td>
</tr>
</tbody>
</table>
A 100-MHz-2-GHz closed-loop analog in-phase/ quadrature correction circuit for digital clocks is presented. The proposed circuit consists of a phase-locked looptype architecture for quadrature error correction. The circuit corrects the phase error to within 1.5° up to 1 GHz and to within 3° at 2 GHz. It consumes 5.4 mA from a 1.2 V supply at 2 GHz. The circuit was designed in UMC 0.13-μm mixed-mode CMOS with an active area of 102 μm×95 μm. The impact of duty cycle distortion has been analyzed. High-frequency quadrature measurement related issues have been discussed. The proposed circuit was used in two different applications for which the functionality has been verified.

A fully integrated step-down switched-capacitor dc-dc converter ring with 123 phases has been designed that could achieve fast dynamic voltage scaling for the microprocessor of wearable devices. The symmetrical multiphase converter ring surrounds its load in the square and supplies power to the on-chip power grid that is easily accessible at any point of the chip edges. The frequency of the VDD-controlled oscillator is adjusted through its supply voltage VDD, which allows the unity-gain frequency to be designed higher than the switching frequency. The converter ring has been fabricated in a low-leakage 65-nm CMOS process. This converter achieves a response time of 3 ns, a reference tracking speed of 2.5 V/μs, and a minimum output ripple of 2.2 mV. The peak efficiency is 80% at the power density of 66.6 mW/mm², and the maximum power density is 180 mW/mm².
<table>
<thead>
<tr>
<th>ETPL VLSI - 027</th>
<th>A 5-Gb/s Digital Clock and Data Recovery Circuit with Reduced DCO Supply Noise Sensitivity Utilizing Coupling Network.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A digital clock and data recovery (CDR) is presented, which employs a low supply sensitivity scheme for a digitally controlled oscillator (DCO). A coupling network comprising capacitors, resistors, and coupling buffers enhances the supply variation immunity of the DCO and mitigates the jitter performance degradation. A supply variation-dependent bias generator produces the corresponding bias voltage to alleviate the supply variation with minimal area and power penalty. The proposed scheme improves 29.3 ps of peak-to-peak jitter and 11.5 dB of spur level, at 6 and 5 MHz 50 mVpp sinusoidal supply noise tone, respectively. Fabricated in a 65-nm CMOS process, the proposed CDR operates at 5-Gb/s data rate with BER ( \times 10^{-12} ) for PRBS 31 and consumes 15.4 mW. The CDR occupies an active die area of 0.075 mm(^2).</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ETPL VLSI - 028</th>
<th>28-nm Latch-Type Sense Amplifier Modification for Coupling Suppression.</th>
</tr>
</thead>
<tbody>
<tr>
<td>With the development of modern semiconductor fabrication technology, the channel length of the CMOS device and the device pitch continually shrink accompanied by more and more severe process variation and signal coupling effect, respectively. In this paper, we explain how the coupling effect interferes with the action of the sense amplifier (SA); then we introduce a coupling suppressed SA. In our design, we adjust the time control. The coupled signals are classified and suppressed by different turn on currents. The new architecture can achieve obvious improvement under differential input in our Monte Carlo simulation. The area and speed cost can be omitted. Through our work, we recommend our design of SA and draw attention to the coupling effect for other circuits.</td>
<td></td>
</tr>
<tr>
<td>ETPL VLSI - 029</td>
<td>10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage.</td>
</tr>
<tr>
<td>----------------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>We present, in this paper, a new 10T static random access memory cell having single ended decoupled read-bitline (RBL) with a 4T read port for low power operation and leakage reduction. The RBL is precharged at half the cell's supply voltage, and is allowed to charge and discharge according to the stored data bit. An inverter, driven by the complementary data node (QB), connects the RBL to the virtual power rails through a transmission gate during the read operation. RBL increases toward the V_DD level for a read-1, and discharges toward the ground level for a read-0. Virtual power rails have the same value of the RBL precharging level during the write and the hold mode, and are connected to true supply levels only during the read operation. Dynamic control of virtual rails substantially reduces the RBL leakage. The proposed 10T cell in a commercial 65 nm technology is 2.47× the size of 6T with β = 2, provides 2.3× read static noise margin, and reduces the read power dissipation by 50% than that of 6T. The value of RBL leakage is reduced by more than 3 orders of magnitude and (I_ON/I_OFF) is greatly improved compared with the 6T BL leakage. The overall leakage characteristics of 6T and 10T are similar, and competitive performance is achieved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>This brief proposes a novel power-gated 9T (PG9T) static random access memory (SRAM) cell that uses a read-decoupled access buffer and power-gating transistors to execute reliable read and write operations. The proposed 9T SRAM cell uses bit interleaving to achieve soft error immunity and utilizes a column-based virtual VSS signal to eliminate unnecessary bitline discharges in the unselected columns, thereby reducing the energy consumption. In a 22-nm FinFET technology, the proposed PG9T SRAM cell has a minimum operating voltage of 0.32 V while achieving the 6σ read stability yield. Compared with the previously proposed 9T SRAM cell, the proposed cell consumes 45% and 17% less energy per read and write operation, respectively, at the minimum operating voltage, and has a 12% smaller bit cell area.</td>
<td></td>
</tr>
</tbody>
</table>
ETPL VLSI - 031 Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications.

The limited size and power budgets of space-bound systems often contradict the requirements for reliable circuit operation within high-radiation environments. In this paper, we propose the smallest solution for soft-error tolerant embedded memory yet to be presented. The proposed complementary dual-modular redundancy (CDMR) memory is based on a four-transistor dynamic memory core that internally stores complementary data values to provide an inherent per-bit error detection capability. By adding simple, low-overhead parity, an error-correction capability is added to the memory architecture for robust soft-error protection. The proposed memory was implemented in a 65-nm CMOS technology, displaying as much as a 3.5×1 smaller silicon footprint than other radiation-hardened bitcells. In addition, the CDMR memory consumes between 48% and 87% less standby power than other considered solutions across the entire operating region.


Pulsed latches are gaining increased visibility in low-power ASIC designs. They provide an alternative sequential element with high performance and low area and power consumption, taking advantage of both latch and flip-flop features. While the circuit reliability and robustness against different process, voltage, and temperature variations are considered as critical issues with current technologies, no significant reliability study was proposed for pulsed latch circuits. In this paper, we present a study on the effect of different PVT variations on the behavior of pulsed latches, considering the effect on both the pulser and the latch. In addition, two novel design approaches are presented to enhance the reliability of pulsed latch circuits, while keeping their main advantages of high performance, low power, and small area. Experiments performed using Synopsys 28nm PDK demonstrate the ability of the proposed approaches to keep the same reliability level at different supply voltages and temperatures in the presence of process variations, with a very small area overhead of around 3%. The two proposed designs have negligible power overhead when running at nominal supply voltage, and they have higher yield per unit power when compared with the traditional design at different voltages and temperatures.
<table>
<thead>
<tr>
<th>ETPL VLSI - 033</th>
<th>Reliability-Tolerant Design for Ultra-Thin-Body GeOI 6T SRAM Cell and Sense Amplifier.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>This paper investigates the reliability-tolerant design for ultra-thin-body (UTB) GeOI 6T SRAM cell and sense amplifiers. For UTB GeOI 6T SRAM cells, using high threshold voltage design significantly mitigates the read and hold static noise margin degradations due to NBTI and PBTI. Due to worse PBTI degradations, as stress (aging) time increases, GeOI current and voltage latch sense amplifiers show larger degradation in word-line to sense amplifier enable (SAE) delay ($T_{WS}$) and sense amplifier sensing delay ($T_{SA}$) compared with the SOI counterparts. Using WL to SAE self-timed sensing scheme mitigates the BTI induced delay degradation. A new reliability-tolerant sense amplifier with speed-up design is proposed for the first time to improve the PBTI dominated sensing delay for UTB GeOI sense amplifier.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ETPL VLSI - 034</th>
<th>RS flip-flop implementation based on all spin logic devices</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>All spin logic (ASL) device is one of the promising post-CMOS candidates. Owing to unique features such as non-volatility, simple configuration, ultra-low-switching energy, and good scalability, ASL devices can be exploited in logic applications. Based on the characteristics of non-volatility and bistable states of ASL device, an RS flip-flop is proposed which is composed of seven ASL devices and employs a complementary clock signal scheme. Using the coupled spin-transport/magneto-dynamics model, validity of its logic operation is demonstrated. As a fundamental building block of sequential logic circuits, the proposed RS flip-flop will be a useful component for designing large-scale ASL sequential logic circuits.</td>
</tr>
</tbody>
</table>
In this study, an area and power-efficient iterative floating-point (FP) multiplier architecture is designed and implemented on FPGA devices with pipelined architecture. The proposed multiplier supports both single-precision (SP) and double-precision (DP) operations. The operation mode can be switched during run time by changing the precision selection signal. The Karatsuba algorithm is applied when mapping the mantissa multiplier in order to reduce the number of digital signal processing (DSP) blocks required. For DP operations, the iterative method is applied which require much less hardware than a fully pipelined DP multiplier and thus reduces the power consumption. To further reduce the power consumption, the unused logic blocks for a specific operation mode are disabled. Compared to previous work, the proposed multiplier can achieve 33% reduction of DSP blocks, 4.3% less look-up tables (LUTs), and 31.2% less flip-flops while having 4% faster clock frequency on Virtex-5 devices. Compared to the intellectual property core DP multiplier provided by the FPGA vendors, the proposed multiplier required less DSP blocks and achieves lower-power consumption. The mapping solutions and implementation results of the proposed multiplier on Xilinx Virtex-7 and Altera Arria-10 devices are also presented. In addition, the results of a direct implementation of the proposed architecture on STM-90 nm ASIC platform are reported.

Among the emerging technologies recently proposed as alternatives to the classic CMOS, quantum-dot cellular automata (QCA) is one of the most promising solutions to design ultralow-power and very high speed digital circuits. Efficient QCA-based implementations have been demonstrated for several binary and decimal arithmetic circuits, but significant improvements are still possible if the logic gates inherently available within the QCA technology are smartly exploited. This brief proposes a new approach to design QCA-based BCD adders. Exploiting innovative logic formulations and purpose-designed QCA modules, computational speed significantly higher than existing counterparts is achieved without sacrificing either the occupied area or the cell count.
This paper introduces a new heuristic to generate pipelined run-time reconfigurable constant multipliers for field-programmable gate arrays (FPGAs). It produces results close to the optimum. It is based on an optimal algorithm which fuses already optimized pipelined constant multipliers generated by an existing heuristic called reduced pipelined adder graph (RPAG). Switching between different single or multiple constant outputs is realized by the insertion of multiplexers. The heuristic searches for a solution that results in minimal multiplexer overhead. Using the proposed heuristic reduces the run-time of the fusion process, which raises the usability and application domain of the proposed method of run-time reconfiguration. An extensive evaluation of the proposed method confirms a 9%–26% FPGA resource reduction on average compared to previous work. For reconfigurable multiple constant multiplication, resource savings of up to 75% can be shown compared to a standard generic lookup table based multiplier. Two low level optimizations are presented, which further reduce resource consumption and are included into an automatic VHDL code generation based on the FloPoCo library.

The Viterbi algorithm is commonly applied to a number of sensitive usage models including decoding convolutional codes used in communications such as satellite communication, cellular relay, and wireless local area networks. Moreover, the algorithm has been applied to automatic speech recognition and storage devices. In this paper, efficient error detection schemes for architectures based on low-latency, low-complexity Viterbi decoders are presented. The merit of the proposed schemes is that reliability requirements, overhead tolerance, and performance degradation limits are embedded in the structures and can be adapted accordingly. We also present three variants of recomputing with encoded operands and its modifications to detect both transient and permanent faults, coupled with signature-based schemes. The instrumented decoder architecture has been subjected to extensive error detection assessments through simulations, and application-specific integrated circuit (ASIC) [32 nm library] and field-programmable gate array (FPGA) [Xilinx Virtex-6 family] implementations for benchmark. The proposed fine-grained approaches can be utilized based on reliability objectives and performance/implementation metrics degradation tolerance.
### ETPL VLSI - 039
A 250-Mb/s to 6-Gb/s Referenceless Clock and Data Recovery Circuit with Clock Frequency Multiplier.

This brief describes the design and implementation of a 250-Mb/s to 6-Gb/s single-loop referenceless clock and data recovery circuit. The clock frequency multiplier and the referenceless frequency acquisition circuit are used to cover a wide-range data rate. The clock frequency multiplier is proposed to generate the 6-GHz clock with low jitter. In addition, the voltage-controlled oscillator operates at 1/5-rate frequency of the sampling clock, which has a merit of low power consumption. The proposed circuit achieves 9.56-ps rms jitter, consumes 13.2 mW at 6 Gb/s, and occupies 0.0944 mm² in a 65-nm CMOS technology.

### ETPL VLSI - 040

This paper proposes a V-band ×8 frequency multiplier for 60-GHz wireless communication systems using 65-nm CMOS technology. The ×8 frequency multiplier consists of three stages of amplifiers and three stages of doublers. The second and fifth stages of the frequency multiplier are balanced structures, while the third stage of the frequency multiplier is a single-ended structure. The proposed ×8 frequency multiplier is optimized, and it has low power consumption, high spectral purity, and a small size. It occupies an area of 1.32 × 0.7 mm² and achieves a maximum output power of -1.8 dBm with an input power of -24 dBm in the frequency range of 46.4-52 GHz. The circuit consumes 55 mA from a 1-V supply. All harmonic suppressions are over 37.6 dBc in the frequency range of 46.4-52 GHz. These results represent the state-of-the-art for CMOS frequency multipliers.
Approximate computing can decrease the design complexity with an increase in performance and power efficiency for error resilient applications. This brief deals with a new design approach for approximation of multipliers. The partial products of the multiplier are altered to introduce varying probability terms. Logic complexity of approximation is varied for the accumulation of altered partial products based on their probability. The proposed approximation is utilized in two variants of 16-bit multipliers. Synthesis results reveal that two proposed multipliers achieve power savings of 72% and 38%, respectively, compared to an exact multiplier. They have better precision when compared to existing approximate multipliers. Mean relative error figures are as low as 7.6% and 0.02% for the proposed approximate multipliers, which are better than the previous works. Performance of the proposed multipliers is evaluated with an image processing application, where one of the proposed models achieves the highest peak signal to noise ratio.

This paper presents the design of approximate 15-4 compressor using 5-3 compressors as basic module. Four different types of approximate 5-3 compressors are used in a 15-4 compressor for less power consumption and high pass rate. We have analysed the results in all the cases. A 16 × 16 bit multiplier is simulated using the proposed 15-4 compressor. Simulation results show that the multipliers with proposed approximate compressors achieve significant improvement in power as compared to the multipliers with accurate 15-4 compressor. Pass rate of the proposed multipliers are high as compared to other existing approximate multipliers. Finally, the proposed multiplier is used in image processing applications, where the peak signal to noise ratio of the image is measured. Quality of the image is compared with an accurate multiplier and the obtained results show that our proposed multiplier performs better than existing approximate multiplier.
### ETPL VLSI - 043
Optimized Memristor-Based Multipliers.

Since memristors came to the forefront of research, minimal work has explored their application to computer arithmetic. This paper proposes two memristor-based implementations of an N-bit shift-and-add multiplier, one using IMPLY operations and a second using MAD operations. The optimized IMPLY-based implementation reduces the baseline delay from $2N^2 + 29N$ steps and $17N+3$ memristors to $2N^2 + 21N$ steps and $7N+1$ memristors. A second implementation is proposed that is constructed from MAD gates, a lower-area, lower-delay alternative to IMPLY logic. This design performs an N-bit multiplication in $N^2 + N$ steps with $5N$ memristors and $3N+2$ drivers. Both designs require fewer steps and less than 1/6 of the number of components of a traditional CMOS design. Finally, both of the implementations are extended to implement radix-2 Booth multipliers. The IMPLY design only increases by 1 step per iteration and 2N memristors and drivers. The MAD design increases by N memristors and 6N switches but maintains the same delay as the shift-and-add multiplier. Both designs maintain a lower area and lower delay than the CMOS equivalent.

### ETPL VLSI - 044
16 × 1 Packaged MUX/DEMUX for Flexible-Grid Optical Networks.

A comprehensive experimental study on the performance of a packaged flexible-grid compliant 16 × 1 packaged MUX/DEMUX device is presented. The device relies on a bandwidth and wavelength selective filtering element array integrated on an SOI platform, equipped with on-chip polarization multiplexing functionality. Multilateral operating credentials are demonstrated through the evaluation of the device in 2 × 1 MUX, 1 × 2 DEMUX and PolMUX configurations scenarios under realistic data traffic conditions, thus confirming its suitability for next-generation flexible-grid optical networks.
A novel method for designing and realising compact digital circuits by engineering MOSFET gate electrode is proposed. The novelty is the use of gate engineered single devices in the pull-up (PU) and pull-down (PD) paths of a static CMOS gate instead of multiple transistors as used in conventional CMOS implementations of circuits. Herein, two input NAND, NOR, and exclusive-OR (XOR) gates employing the proposed gate engineering concept are designed and simulated. Engineered gate N-type MOS and P-type MOS are used for PD and pull-up circuits, respectively. Since only two devices are used for a complete circuit: one in PU network and other in PD network; therefore, area and power of the proposed circuits get reduced significantly in comparison with the conventional static CMOS circuits. Mixed mode simulations have shown that the proposed technique realises NAND, NOR and XOR operations perfectly and it can be extended to realise other combinational and sequential circuits easily.

With fabrication technology reaching nanolevels, systems are becoming more prone to manufacturing defects with higher susceptibility to soft errors. This paper is focused on designing combinational circuits for soft error tolerance with minimal area overhead. The idea is based on analyzing random pattern testability of faults in a circuit and protecting sensitive transistors, whose soft error detection probability is relatively high, until desired circuit reliability is achieved or a given area overhead constraint is met. Transistors are protected based on duplicating and sizing a subset of transistors necessary for providing the protection. In addition to that, a novel gate-level reliability evaluation technique is proposed that provides similar results to reliability evaluation at the transistor level (using SPICE) with the orders of magnitude reduction in CPU time. LGSynth'91 benchmark circuits are used to evaluate the proposed algorithm. Simulation results show that the proposed algorithm achieves better reliability than other transistor sizing-based techniques and the triple modular redundancy technique with significantly lower area overhead for 130-nm process technology at a ground level.
This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2-4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed by using mixed-logic 2-4 predecoders combined with standard CMOS postdecoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

In this paper, the classical CMOS Schmitt trigger (ST) operating in the subthreshold regime is analyzed. The complete DC voltage transfer characteristic of the CMOS ST is determined. The metastable segment of the characteristic is explained in terms of the negative resistance of the NMOS and PMOS subcircuits of the ST. Small-signal analysis is carried out to determine the minimum supply voltage at which the hysteresis appears and to obtain a rough estimation of the hysteresis width. It is shown that the theoretical minimum supply voltage required to obtain hysteresis is $2\ln(2 + \sqrt{5})kT/q = 75$ mV at room temperature. A test chip with CMOS Schmitt triggers was designed and fabricated in a 180 nm technology in order to study their operation at supply voltages between 50 mV and 1000 mV.
This brief introduces a highly configurable ultrawideband triangular wave baseband pulse generator designed in 40-nm complementary metal-oxide-semiconductor technology. The baseband pulse width is adjustable between 660 ps and 3.8 ns. An extra amplitude compensation loop is implemented to prevent amplitude changes when the pulse width varies. The amplitude variations are limited to 13% compared with the maximum amplitude over the entire pulse width range. The amplitude compensation loop allows a pulse amplitude tuning range between 280 and 640 mV, whereas the pulse width only varies 80 ps over this entire range. The pulse generator has a maximum simulated signal-to-noise ratio of 59 dB and a measured maximum power consumption of 6.2 pJ/pulse from a 0.9-V power supply and a 100-MHz pulse repetition frequency.

We present a study of dual-band injection locking frequency dividers (ILFDs), based on a nonlinear analysis. We develop a quasi-normal model of these dividers suitable for applying the method of averaging, which allowed us to derive in a simple and expressive manner the first-approximation equations for the amplitudes and phases of the locked modes, both in transient and in steady state. The phase equations have the same form of the Adler's equation, and represent the generalization of that well-known equation to higher-order frequency dividers. These equations allowed us to derive the locking ranges in a simple explicit form, useful for design purposes. The theoretical results are validated by Spice simulations, and by measurements on a circuit prototype.

We present the design of readout circuitry based on complementary metal-oxide semiconductors (CMOS) for spin-waves. The circuit provides the functionality of a high-speed oscilloscope/spectrum analyzer, and can be integrated with a spin-wave-based signal processing device. The circuit consumes sub-50 mW power and requires an area below 1 mm². A spin-wave-based processing system, when combined with the presented electrical input/output circuitry, can perform complex microwave signal processing tasks, with speed, power consumption, and area that are not feasible in a CMOS-only system.
Thank you!